

ABSTRACT

A memory array comprising nanoscale wires is disclosed. The nanoscale wires are addressed by means of controllable regions axially and/or radially distributed along the nanoscale wires. In a one-dimensional embodiment, memory locations are defined by crossing points between nanoscale wires and microscale wires. In a two-dimensional embodiment, memory locations are defined by crossing points between perpendicular nanoscale wires. In a three-dimensional embodiment, memory locations are defined by crossing points between nanoscale wires located in different vertical layers.